FIGURE 1A

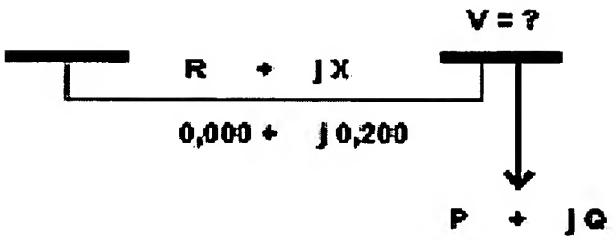


FIGURE 1B

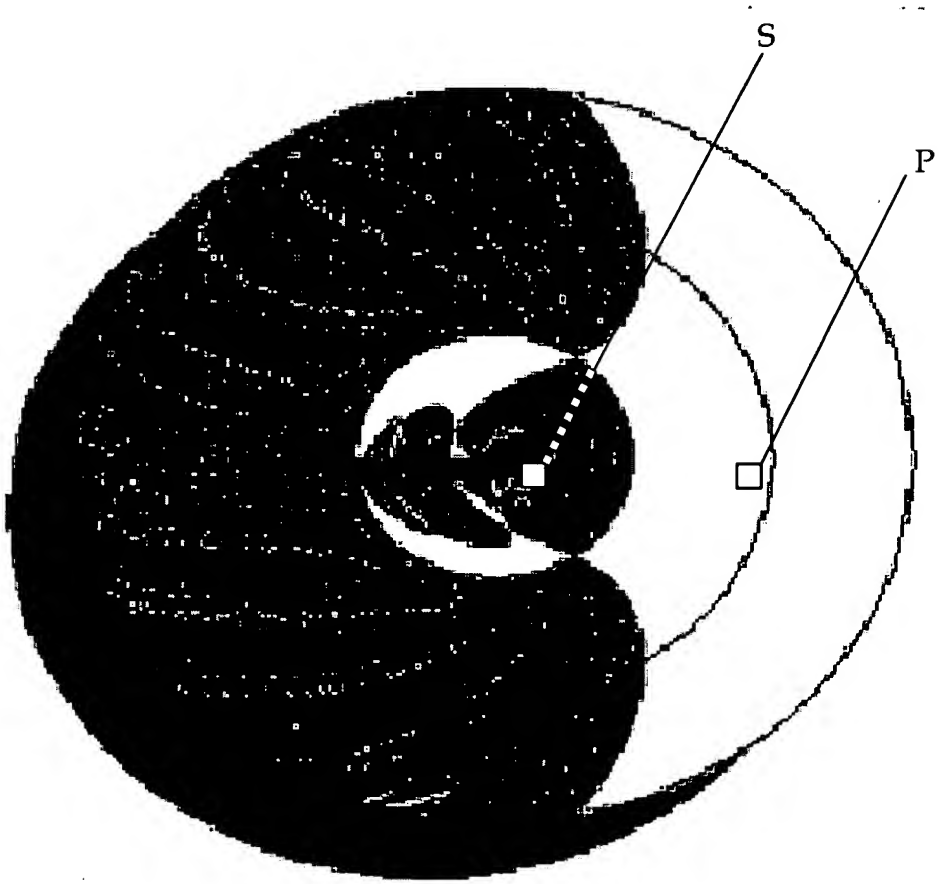


FIGURE 1C

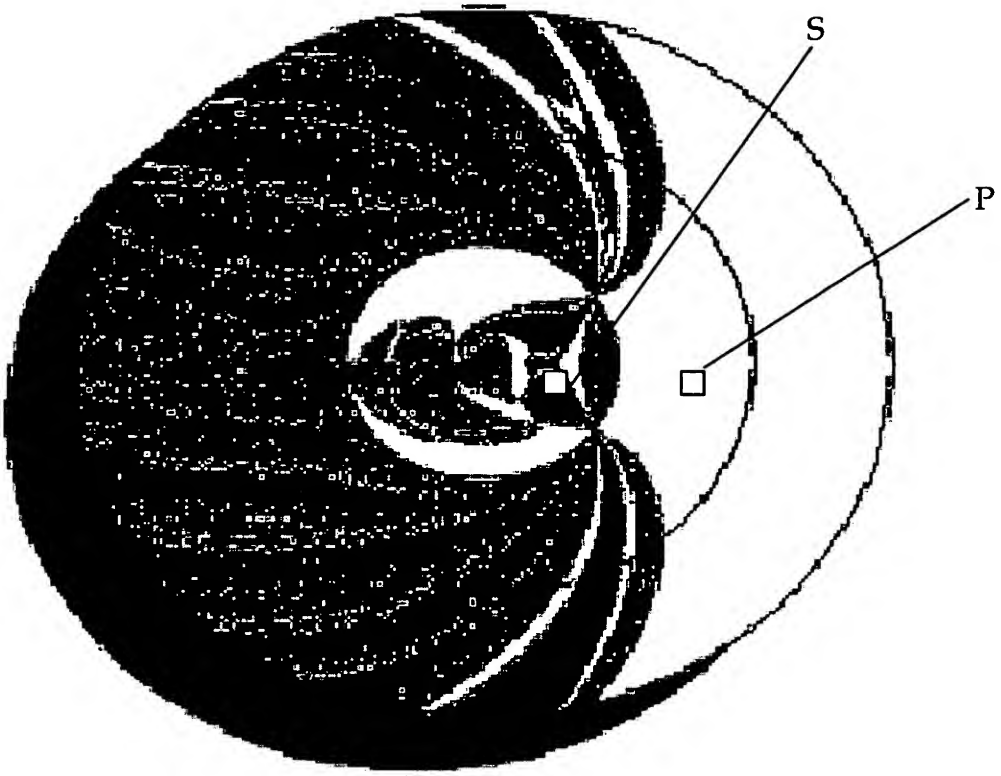


FIGURE 1D

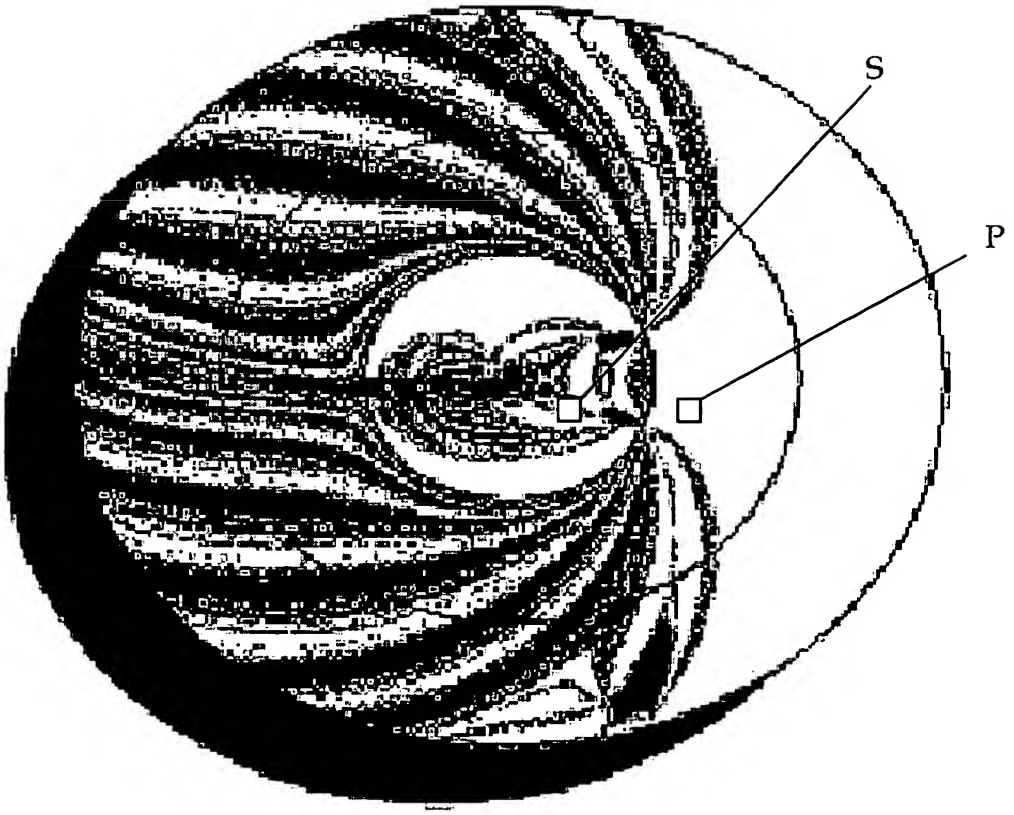


FIGURE 1E

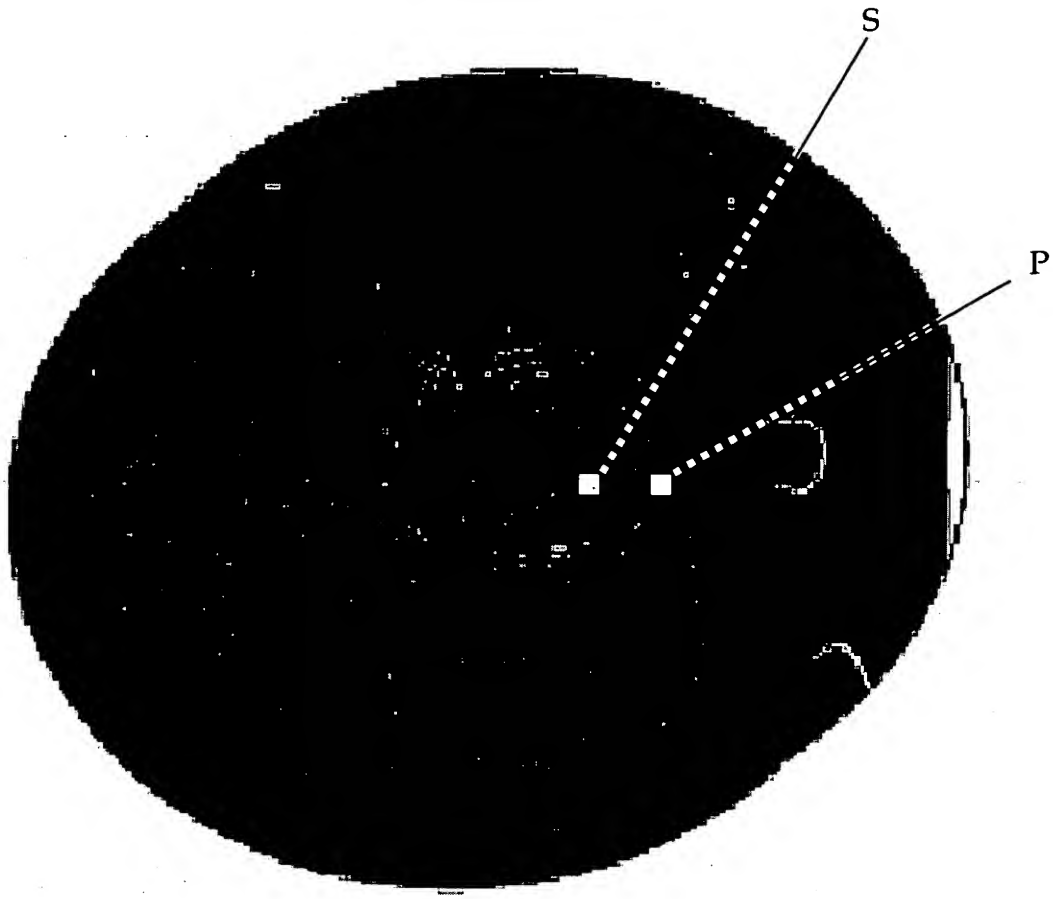


FIGURE 2

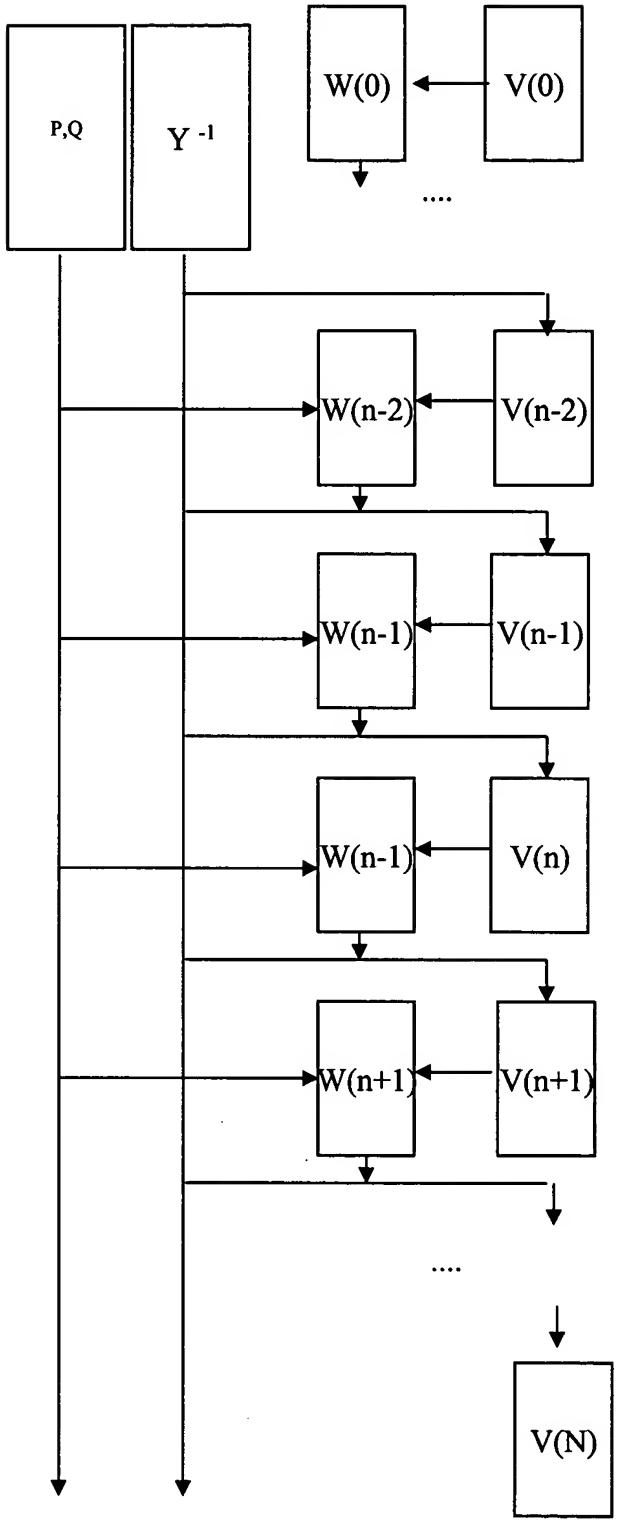


FIGURE 3

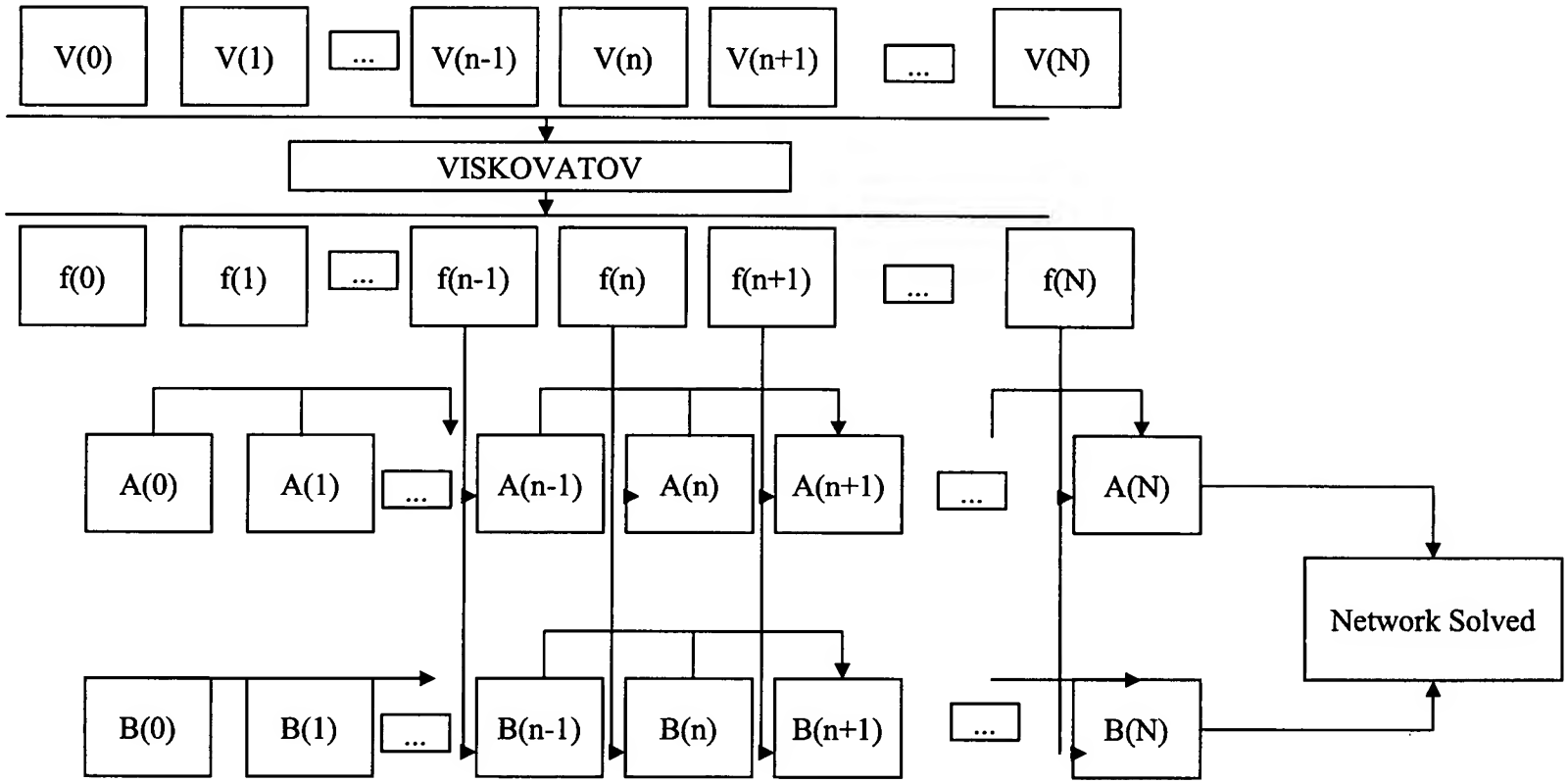
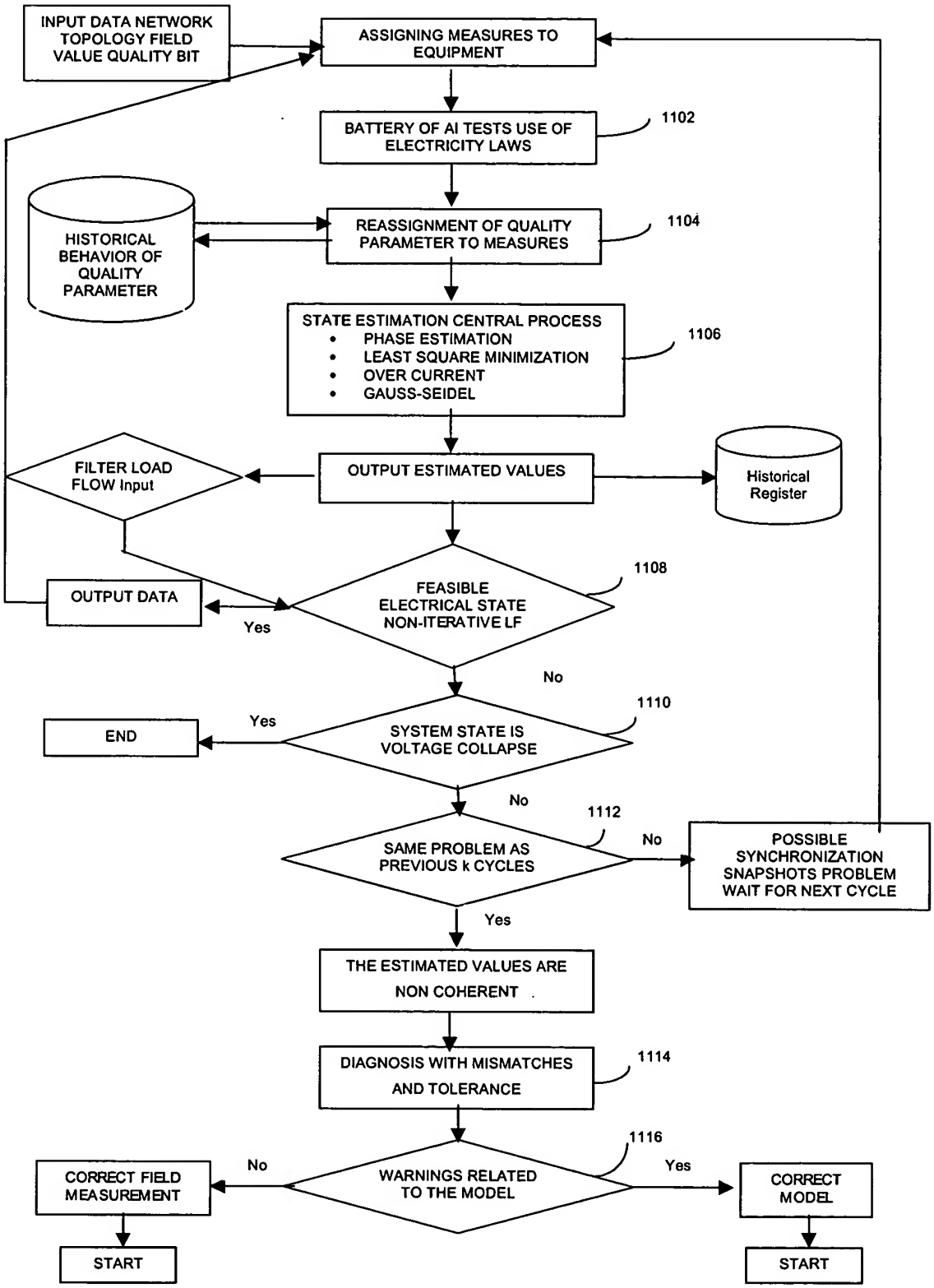

V(0)
V(1)
...
V(n-1)
V(n)
V(n+1)
...
V(N)
VISKOVATOV
f(0)
f(1)
...
f(n-1)
f(n)
f(n+1)
...
f(N)
A(0)
A(1)
...
A(n-1)
A(n)
A(n+1)
...
A(N)
Network Solved
B(0)
B(1)
...
B(n-1)
B(n)
B(n+1)
...
B(N)

FIGURE 4


INPUT DATA NETWORK TOPOLOGY FIELD VALUE QUALITY BIT
ASSIGNING MEASURES TO EQUIPMENT
BATTERY OF AI TESTS USE OF ELECTRICITY LAWS
1102
HISTORICAL BEHAVIOR OF QUALITY PARAMETER
REASSIGNMENT OF QUALITY PARAMETER TO MEASURES
1104
STATE ESTIMATION CENTRAL PROCESS
• PHASE ESTIMATION
• LEAST SQUARE MINIMIZATION
• OVER CURRENT
• GAUSS-SEIDEL
1106
FILTER LOAD FLOW Input
OUTPUT ESTIMATED VALUES
Historical Register
OUTPUT DATA
Yes
FEASIBLE ELECTRICAL STATE NON-ITERATIVE LF
1108
No
END
Yes
SYSTEM STATE IS VOLTAGE COLLAPSE
1110
No
SAME PROBLEM AS PREVIOUS k CYCLES
1112
No
POSSIBLE SYNCHRONIZATION SNAPSHOTS PROBLEM WAIT FOR NEXT CYCLE
Yes
THE ESTIMATED VALUES ARE NON COHERENT
DIAGNOSIS WITH MISMATCHES AND TOLERANCE
1114
WARNINGS RELATED TO THE MODEL
1116
No
Yes
CORRECT FIELD MEASUREMENT
CORRECT MODEL
START
START